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EXAMINER	
UNELUS, ERNEST	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,326	DICKENS ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1-6, 8-17, and 19-31*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-17 and 19-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03/29/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Applicant's arguments with respect to claims 1-6, 8-17, and 19-31 have been considered but are moot in view of the new ground(s) of rejection

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

III. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1, 4-6, 8-12, 15-17, 19-23, and 26-31,** are rejected under 35 U.S.C. 102(e) as being anticipated by Grun (US pat. 6,629,166).

6. As per **claim 1**, Grun discloses "A method, comprising:

signaling **(which also means to select, as discloses by the applicant on page 5, paragraph 0014)**, as part of a diagnostic operation with respect to an Input/Output (I/O) controller **(see col. 10, lines 15-23, which discloses diagnostic primitive operation)**, a reconnection inhibitor **(Target Channel Adapter 22 of fig. 2)** over a bus **(see bus connection between the adapter and the I/O controller 24 of fig. 2)** to cause the reconnection inhibitor to access the bus to inhibit an Input/Output (I/O) controller from accessing the bus **(see col. 11, lines 12-14, which discloses "Upon completion of the transfer, the I/O controller may then send a message to the initiator notifying the initiator that the information transfer has been completed". Therefore, while the channel adapter transfer data from the initiator to the controller, the controller is block from transfer data to the initiator. Indirectly, the adapter**

blocks the controller from transferring. See also col. 9, lines 52-55 and fig. 2 for further detail); and

transmitting, as part of a diagnostic operation, by an initiator, I/O requests on the bus to the I/O controller, wherein the I/O requests are queued in an I/O queue **(see col. 11, lines 27-33, which discloses "Prior to receiving a message, such as an I/O service request from an initiator, an I/O controller may allocate buffers to receive those inbound messages. Having allocated one or more message buffers, an I/O controller may then pass pointers to those buffers and thus control of the buffers to a message and data service using a target service interface primitive")**; wherein the I/O controller is inhibited by the reconnection inhibitor from draining while the initiator transmits requests to the I/O controller **(see col. Lines 52-55 and col. 11, lines 12-14 and fig. 2, which discloses, as the controller uses the target adapter to receive data, it only respond or transfer after it receive, not while it's receiving. The target adapter serves as a kind of blocking device because it can only transfer into or out of the controller at a time, not both at the same time)**; and

performing diagnostic testing of the I/O controller when the I/O queue is at different levels **(see col. 12, line 62 to col. 13, line 42, which discloses an initial primitive diagnostic of a newly controller or a returning controller that has to go through a reset. Therefore, the initialization of a returning controller will consist of this controller's queue being in a different level compare to when it was first connected to the system. See col. 8, line 55 to col. 9, line 5 for further detail. Also, the queue of a current controller in the system will be at different levels when a newly controller is dynamically added to the system; see col. 13 line 43 to col. 14, line 15)**, wherein the level of I/O requests pending in the I/O queue is

controlled by the signaling of the reconnection inhibitor **(as the target channel adapter transfer requests from and to the controller, it's indirectly controlling the queue inside the controller; see fig. 2 and col. 10, lines 24-30).**

7. As per **claim 12**, Grun discloses "A system, comprising:

a reconnection inhibitor **(Target Channel Adapter 22 of fig. 2)**; an initiator **(Initiator 20 of fig. 2)**; an Input/Output (I/O) controller **(I/O controller 24 of fig. 2)**; a bus **(see bus connection between the adapter and the I/O controller 24 of fig. 2)**, wherein the reconnection inhibitor, initiator, and the I/O controller communicate over the bus **(see fig. 2)**; circuitry in the initiator capable of causing operations comprising **(all electric devices are function by electric circuitry)**:

(i) signaling **(which also means to select, as discloses by the applicant on page 5, paragraph 0014),** as part of a diagnostic operation with respect to an Input/Output (I/O) controller **(see col. 10, lines 15-23, which discloses diagnostic primitive operation)**, the reconnection inhibitor over the bus **(see fig. 2)**; and

(ii) transmitting, as part of a diagnostic operation, I/O requests on the bus to the I/O controller after signaling the reconnection inhibitor **(see col. 11, lines 27-33, which discloses "Prior to receiving a message, such as an I/O service request from an initiator, an I/O controller may allocate buffers to receive those inbound messages. Having allocated one or more message buffers, an I/O controller may then pass pointers to those buffers and thus control of the buffers to a message and data service using a target service interface primitive")**; and

(iii) performing diagnostic testing of the I/0 controller when the I/0 queue is at different levels **(see col. 12, line 62 to col. 13, line 42, which discloses an initial primitive diagnostic of a newly controller or a returning controller that has to go through a reset. Therefore, the initialization of a returning controller will consist of this controller's queue being in a different level compare to when it was first connected to the system. See col. 8, line 55 to col. 9, line 5 for further detail. Also, the queue of a current controller in the system will be at different levels when a newly controller is dynamically added to the system; see col. 13 line 43 to col. 14, line 15)**, wherein the level of I/0 requests pending in the I/0 queue is controlled by the signaling of the reconnection inhibitor **(as the target channel adapter transfer requests from and to the controller, it's indirectly controlling the queue inside the controller; see fig. 2 and col. 10, lines 24-30)**; and

circuitry in the reconnection inhibitor capable of accessing the bus to inhibit the Input/Output (I/O) controller from accessing the bus in response to receiving the signal from the initiator **(see col. 11, lines 12-14, which discloses "Upon completion of the transfer, the I/O controller may then send a message to the initiator notifying the initiator that the information transfer has been completed". Therefore, while the channel adapter transfer data from the initiator to the controller, the controller is block from transfer data to the initiator. Indirectly, the adapter blocks the controller from transferring. See also col. 9, lines 52-55 and fig. 2 for further detail)**, wherein the I/O requests transmitted by the initiator are queued in an I/O queue **(see col. 11, lines 27-33 and fig. 6)**, wherein the I/O controller is inhibited by the reconnection inhibitor from draining the queue while the initiator transmits requests to the I/O controller **(see col. Lines 52-55 and col. 11, lines 12-14 and fig. 2, which**

discloses, as the controller uses the target adapter to receive data, it only respond or transfer after it receive, not while it's receiving. The target adapter serves as a kind of blocking device because it can only transfer into or out of the controller at a time, not both at the same time).

8. As per **claims 4, 15, and 26**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein the initiator signals the reconnection inhibitor to arbitrate on the bus when a device other than the initiator is arbitrating on the bus **(see 9, lines 40-63)**.

9. As per **claims 5, 16, and 27**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, further comprising signaling the reconnection inhibitor to cease accessing the bus, wherein the I/O controller accesses the bus to complete processing of an I/O request and process further I/O requests in the I/O queue in response to the reconnection inhibitor ceasing to issue requests on the bus" **(see col. 11, lines 12-14, which discloses "Upon completion of the transfer, the I/O controller may then send a message to the initiator notifying the initiator that the information transfer has been completed". Therefore, while the channel adapter transfer data from the initiator to the controller, the controller is block from transfer data to the initiator. Indirectly, the adapter blocks the controller from transferring. See also col. 9, lines 52-55 and fig. 2 for further detail)**.

10. As per **claims 6, 17, and 28**, Grun discloses "The method of claim 5," **[See rejection to claim 5 above]**, wherein the level of I/O requests pending in the I/O queue is controlled by

signaling the reconnection inhibitor, wherein the I/O queue is increased by signaling the reconnection inhibitor to access the bus to inhibit the I/O controller from accessing the bus and depleting the I/O queue, and wherein the I/O queue is decreased by signaling the reconnection inhibitor to cease accessing the bus to inhibit the I/O controller **(see fig. 6 and col. Lines 52-55 and col. 11, lines 12-14, which discloses, as the controller uses the target adapter to receive data, it only respond or transfer after it receive, not while it's receiving. The target adapter serves as a kind of blocking device because it can only transfer into or out of the controller at a time, not both at the same time)**.

11. As per **claims 8, 19, and 29**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein the reconnection inhibitor accesses the bus to inhibit the I/O controller when the I/O controller attempts to arbitrate on the bus **(see 9, lines 40-63)**.

12. As per **claims 9, 20, and 30**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein the reconnection inhibitor inhibits the I/O controller from processing further I/O requests in the I/O queue by preventing the I/O controller from communicating with the initiator over the bus to complete I/O requests **(see 9, lines 40-63 and fig. 2)**.

13. As per **claims 10, 21, and 31**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein the I/O controller comprises a storage controller **(Target service interface 26 of fig. 2; see col. 7, lines 26-28, which discloses "A target service interface according to the present invention defines how messages and data are transferred between**

an I/O controller and an initiator"), and wherein the I/0 requests comprise read and write requests directed to a storage system managed by the I/0 controller **(see col. 11, lines 12-14)**.

14. As per **claims 11 and 22**, Grun discloses "The method of claim 1," **[See rejection to claim 1 above]**, wherein the bus comprises a SCSI parallel bus" **(see col. 23, lines 17-25)**.

15. As per **claim 23**, Grun discloses "A device **(Target Channel Adapter 22 of fig. 2)** in communication with an initiator **(Initiator 20 of fig. 2)** and an Input/Output (I/O) controller **(I/O Controller 24 of fig. 2)** over a bus **(see bus connection between the adapter and the I/O controller 24 of fig. 2)**, wherein the device includes circuitry capable of causing operations comprising **(all electric devices are function by electric circuitry)**:

receiving, as part of a diagnostic operation with respect to the I/O controller **(see col. 10, lines 15-23, which discloses diagnostic primitive operation)**, a signal **(which also means to select, as discloses by the applicant on page 5, paragraph 0014)** from the initiator **(see fig. 2)**;

and accessing the bus to inhibit the Input/Output (I/O) controller from accessing the bus in response to the signal, wherein the initiator transmits, as part of the diagnostic operation, I/0 requests on the bus to the I/0 controller **(see col. 11, lines 12-14, which discloses "Upon completion of the transfer, the I/O controller may then send a message to the initiator notifying the initiator that the information transfer has been completed". Therefore, while the channel adapter transfer data from the initiator to the controller, the controller is block from transfer data to the initiator. Indirectly, the adapter blocks the controller from transferring. See also col. 9, lines 52-55 and fig. 2 for further detail)**, wherein the I/0 requests

are queued in an I/0 queue **(see col. 11, lines 27-33 and fig. 6)**, wherein the I/0 controller is inhibited by the device from draining the queue while the initiator transmits requests to the I/0 controller **(see col. Lines 52-55 and col. 11, lines 12-14 and fig. 2, which discloses, as the controller uses the target adapter to receive data, it only respond or transfer after it receive, not while it's receiving. The target adapter serves as a kind of blocking device because it can only transfer into or out of the controller at a time, not both at the same time)**, wherein the initiator performs diagnostic testing of the I/0 controller when the I/0 queue is at different levels **(see col. 12, line 62 to col. 13, line 42, which discloses an initial primitive diagnostic of a newly controller or a returning controller that has to go through a reset. Therefore, the initialization of a returning controller will consist of this controller's queue being in a different level compare to when it was first connected to the system. See col. 8, line 55 to col. 9, line 5 for further detail. Also, the queue of a current controller in the system will be at different levels when a newly controller is dynamically added to the system; see col. 13 line 43 to col. 14, line 15)**, and wherein the level of I/0 requests pending in the I/0 queue is controlled by the device inhibiting the I/0 controller from accessing the bus **(as the target channel adapter transfer requests from and to the controller, it's indirectly controlling the queue inside the controller; see fig. 2 and col. 10, lines 24-30)**.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. **Claims 2, 3, 13, 14, 24, and 25**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Grun (US pat. 6,629,166) in view of Downer et al. (US pat. 6,223,244).

18. As per **claims 2, 13, and 24**, Grun discloses discloses "The method of claim 1," **[See rejection to claim 1 above]**, but fails to disclose expressly wherein the initiator accesses the bus at a higher priority than the reconnection inhibitor, and wherein the reconnection inhibitor accesses the bus at a higher priority than the I/O controller.

However, **(see page 1, paragraph 0003, on the applicant specification, which discloses, "*initiator 4 is assigned the highest SCSI device address, address seven*". Page 7, paragraph 0019 also discloses "*where the test initiator 38 may assert bus address 7 to select the reconnection inhibitor 36, which may be bus address 6*". Similarly, in col. 1, lines 56-65, Downer discloses, "Each SCSI device has a unique bus ID which users set using switches, jumpers, or set-up routines. SCSI IDs range from seven (highest priority device ID) to zero (lowest priority device ID) for regular SCSI and up to 15 for the Wide SCSI variation. With wide SCSI the priority is from seven (highest priority device ID) to zero followed by 15 to eight (lowest priority device ID). Hosts typically have the highest SCSI bus ID, allowing them to initiate requests with minimum peripheral device interference". Therefore, SCSI Controllers 14-18 can be serves as an initiator, a reconnection inhibiter, and an I/C controller)**, and wherein the reconnection inhibitor accesses the bus at a higher priority than the I/O controller **(with respect to what is discloses above, Host computer 14 in**

fig. 1, the reconnection inhibitor will be assigned a SCSI ID of 6, which gives it a higher priority than the I/O controller (Host computer 18 in fig. 1). The I/O controller will be assigned with the next level priority, which will be 5).

Grun (US pat. 6,629,166) and Downer et al. (US pat. 6,223,244) are analogous art because they are from the same field of endeavor of peripheral storage devices connected on an SCSI bus.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a method for interfacing at least one Input/Output (I/O) controller to a channel-based switched fabric that includes: providing at least one channel adapter where the at least one channel adapter allows connection of the at least one I/O controller to a channel-based switched fabric and the at least one channel adapter supports transferring of messages and/or data between the at least one I/O controller and at least one initiating unit connected to the channel-based switched fabric; providing a physical interface between the at least one I/O controller and the at least one channel adapter; and defining a set of command primitives where the command primitives communicate information between the at least one I/O controller and the at least one channel adapter via the physical interface as described by Grun and the method is described and shown herein for assuring device access to a bus having a fixed priority arbitration scheme such as a SCSI bus as taught by Downer

The motivation for doing so would have been because Downer teaches that **"An objective of the invention, therefore, is to provide an efficient method for assuring bus access to all devices connected to a bus having a fixed priority arbitration scheme. Another**

objective of the invention is to assure that lower-priority devices have access to a minimum "fair share" of the bus bandwidth" (see col. 2, lines 36-41).

Therefore, it would have been obvious to combine Downer et al. (US pat. 6,223,244) with Grun (US pat. 6,629,166) for the benefit of creating the method to obtain the invention as specified in claims 2,13, and 24.

19. As per **claims 3, 14, and 25**, the combination of Grun and Downer discloses "The method of claim 2," **[See rejection to claim 2 above]** Downer further discloses "wherein the initiator uses a first device identifier to communicate with the bus **(page 1, paragraph 0003, on the applicant specification discloses "*initiator 4 is assigned the highest SCSI device address, address seven*". Page 7, paragraph 0019 also discloses "*where the test initiator 38 may assert bus address 7 to select the reconnection inhibitor 36, which may be bus address 6*". Similarly, in col. 1, lines 56-65, Downer discloses, "Each SCSI device has a unique bus ID which users set using switches, jumpers, or set-up routines. SCSI IDs range from seven (highest priority device ID) to zero (lowest priority device ID) for regular SCSI and up to 15 for the Wide SCSI variation. With wide SCSI the priority is from seven (highest priority device ID) to zero followed by 15 to eight (lowest priority device ID). Hosts typically have the highest SCSI bus ID, allowing them to initiate requests with minimum peripheral device interference"). With respect to what is discloses above, Host computer 16 in fig. 1, the reconnection inhibitor will be assigned a SCSI ID of 6, which gives it a higher priority than the I/O controller (Host computer 18 in fig. 1). The I/O controller will be assigned with the next level priority, which will be 5),** the reconnection inhibitor uses a second device identifier

to communicate with the bus **(see above)**, and the I/O controller uses a third device identifier to communicate with the bus **(see above)**, wherein the first device identifier has priority over the second device identifier **(see above)**, and wherein the second device identifier has priority over the third device identifier **(see above)**.

V. RELEVANT ART CITED BY THE EXAMINER

20. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

21. The following reference teaches fixed priority arbitration on a bus.

U.S. PATENT NUMBER

US 2005/0283541

US 7,127,572

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

22. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

23. Per the instant office action, claims 1-6, 8-17, and 19-31 have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

25. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 30, 2007

Ernest Unelus
Examiner,
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER